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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,101	06/15/2005	Martijn Henri Richard Lankhorst	NL03 1068 US	7144
24738	7590	05/11/2006		EXAMINER
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131				BUDD, PAUL A
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 05/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)
	10/539,101	LANKHORST ET AL.
	Examiner	Art Unit
	Paul A. Budd	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 15 June 2005.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-12 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-4, 6 and 8-11 is/are rejected.
- 7) Claim(s) 5, 7 and 12 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 15 June 2005 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>6/15/2006</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "122" has been used to designate two separate structures in Figures 2 and 4. In addition, element "125" exists in applicant's disclosure but is never shown in any drawing. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: on page 11 line 24, please change "underetch" to - *-undercut-*. English speaking engineers refer to the isotropic etch process structure described as *undercut*, not underetch. English speaking engineers construe "underetch" to mean incomplete etching, which would have never reached the bottom of the resistor layer 107.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 3 that recites, "heating elements electrical resistance is larger than 0.3 times the minimum of the first electrical resistance and the second electrical resistance" it is unclear if: 1) the limitation is 0.3 times the sum of the two resistances, 2) if the limitation is 0.3 times either of the resistances, 3) if the limitation is 0.3 times only one of the resistances. For the purposes of this office action the examiner will assume that the limitation means that *the heating element's electrical resistance is greater than 0.3 times the lowest resistance state of the resistor comprising a phase change material being changeable between a first phase and a second phase.*

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2,8-9 are rejected under 35 U.S.C. 102 (e) as being anticipated by Moore et al. (US Pat. Pub. 2003/00964497).

Regarding claim 1, Moore teaches an electric device [FIG. 2D] with a body having a resistor [214] comprising a phase change material [page 3, section 0028] being changeable between a first phase [low resistance] and a second phase [high resistance], the resistor [214] having a first electrical resistance [10,000 Ohms, page 4, section 0035] when the phase change material is in the first phase, and a second electrical resistance [10 megaohms, page 4, section 0035], different from the first electrical resistance, when the phase change material is in the second phase, the phase change material constituting a conductive path [FIG. 2D, 226] between a first contact area [212] and a second contact [216'] area a cross-section of the conductive path being smaller [see FIG. 2D, 226] than the first contact area [212] and the second contact area [216'].

Regarding claim 2, Moore teaches an electric device as claimed in claim 1, wherein a part of the conductive path having said cross-section constitutes a volume of phase change material, the volume having an electrical resistance [10,000 ohms] which is larger than an electrical contact resistance at the first

contact area [216'-214] and/or at the second contact area [212-214] independent of whether the phase change material is in the first phase or the second phase. While not stated explicitly the contact structures inherently have a resistance far lower than 10,000 ohms. Official notice is taken with regards to claim 2.

Regarding claim 8, Moore teaches an electric device [FIG. 2D] as claimed in claim 1, wherein the resistor [206] constitutes a memory element [FIG. 4, 416], and the body comprises:

an array of memory cells [FIG. 4], each memory cell [FIG 4, 402] comprising a respective memory element [416] and a respective selection device [404], and a grid of selection lines [408, 412], each memory cell [402] being individually accessible via the respective selection lines [408, 412] connected to the respective selection device [404].

Regarding claim 9, Moore teaches an electric device [FIG. 2D] as claimed in claim 8, wherein:

the selection device [404] comprises a metal oxide semiconductor field effect transistor [page 4, section 0036] having a source region [410], a drain region [414] and a gate region [406], and

the grid of selection lines [408, 412] comprises N first selection lines [see FIG. 4], M second selection lines [see FIG. 4], and an output line [ground], the resistor [416's 206] of each memory element [416] electrically connecting a first region [414] selected

from the source region [410] and the drain region [414] of the corresponding metal oxide semiconductor field effect transistor [404] to the output line [ground], a second region [410] of the corresponding metal oxide semiconductor field effect transistor [404] selected from the source region [410] and the drain region [414] and being free from contact with the first region [separated by the transistor channel], being electrically connected to one of the N first selection lines [412], the gate region [406] being electrically connected to one of the M second selection lines [408].

5. **Claims 1-2,8,10** are rejected under 35 U.S.C. 102 (e) as being anticipated by Van Brocklin et al. (US Patent 6,870,751).

Regarding claim 1, Van Brocklin teaches an electric device [FIG. 3] with a body having a resistor [FIG. 3, 204; column 5 lines 44-45, "change the phase of, or otherwise change the state of the storage element 204] comprising a phase change material [columns 3-4, lines 45-68 and lines 1-11] being changeable between a first phase [amorphous, high resistance] and a second phase [crystalline, low resistance], the resistor [204] having a first electrical resistance [high] when the phase change material is in the first phase, and a second electrical resistance [low], different from the first electrical resistance, when the phase change material [204] is in the second phase [crystalline], the phase change material constituting a conductive path [FIG. 3, the area defined between the dashed lines; column 6, lines 20-34] between a first contact area [106] and a second contact [202, 206] area a cross-section of the conductive path being

smaller [see FIG. 3, between dashed lines] than the first contact area [106] and the second contact area [202, 206].

Regarding claim 2, Van Brocklin teaches an electric device [FIG. 3] as claimed in claim 1, wherein a part of the conductive path having said cross-section constitutes a volume of phase change material [FIG. 3, the volume defined between the dashed lines; column 6, lines 20-34], the volume having an electrical resistance [low or high] which is larger than an electrical contact resistance at the first contact area [106] and/or at the second contact area [202, 206] independent of whether the phase change material is in the first phase or the second phase. While not stated explicitly the contact structures inherently have a resistance far lower than the crystalline phases resistance. Official notice is taken with regards to claim 2.

Regarding claim 8, Van Brocklin teaches an electric device [FIG. 3] as claimed in claim 1, wherein the resistor [204] constitutes a memory element [as above], and the body comprises:

an array of memory cells [FIG. 1], each memory cell [104] comprising a respective memory element and a respective selection device [FIG 2, 200, columns 4-5, lines 44-68 and lines 1-14], and

a grid of selection lines [FIG. 1,106,108], each memory cell [104] being individually accessible via the respective selection lines [106, 108] connected to the respective selection device [200].

Regarding claim 10, Van Brocklin teaches a method of manufacturing an electric device as claimed in Claim 1, comprising the steps of providing a main surface of a pre-fabricated electric device with a layer of the phase change material [204], and reducing a cross-section of a conductive path [see FIG. 3, between dashed lines] in the layer [204] between a first contact area [FIG. 3, 106 to 204] and a second contact area [FIG. 3, specifically 206 to 204] the cross-section [see FIG. 3, between dashed lines] being smaller than the first contact area and the second contact area. Van Brocklin documents a process by which the protrusion 206 is fabricated which creates the “reduced cross-section of a conductive path” which is a small section of the entire 204 volume [column 5, lines 55-61].

6. Claims 1-3,7,10-11 are rejected under 35 U.S.C. 102 (e) as being anticipated by Chiang (US Pat. Pub. 2003/0151041).

Regarding claim 1, Chiang teaches an electric device [FIG. 7] with a body having a resistor [18] comprising a phase change material [18, page 1, section 0002-0005] being changeable between a first phase [amorphous, high resistance] and a second phase [crystalline, low resistance], the resistor [18]

having a first electrical resistance [high] when the phase change material [18] is in the first phase, and a second electrical resistance [low], different from the first electrical resistance, when the phase change material [18] is in the second phase , the phase change material constituting a conductive path [between the spacers, 24] between a first contact area [13 to (24 & 22)] and a second contact area [18-20] a cross-section of the conductive path being smaller [between the spacers, 24] than the first contact area [13 to (24 & 22)] and the second contact area [between the spacers, 24].

Regarding claim 2, Chiang teaches an electric device [FIG. 7] as claimed in claim 1, wherein a part of the conductive path having said cross-section constitutes a volume of phase change material [FIG. 7, the volume defined between the spacers], the volume having an electrical resistance [low or high] which is larger than an electrical contact resistance at the first contact area [13 to (24 & 22)] and/or at the second contact area [18-20] independent of whether the phase change material is in the first phase or the second phase. While not stated explicitly the contact structures inherently have a resistance far lower than the crystalline phases resistance. Official notice is taken with regards to claim 2.

Regarding claim 3, Chiang teaches an electric device [FIG. 7] as claimed in claim 1, further comprising a heating element [FIG. 7, 22] able to conduct an

electric current for enabling a transition from the first phase to the second phase [page 2, section 0026].

Regarding claim 7, Chiang teaches an electric device [FIG. 7] as claimed in claim 3, wherein the heating element [22] is in direct contact with the resistor [See FIG. 7, 18].

Regarding claim 10, Chiang teaches a method of manufacturing an electric device as claimed in Claim 1, comprising the steps of providing a main surface of a pre-fabricated electric device with a layer of the phase change material [18], and reducing a cross-section of a conductive path [see FIG. 7, between the spacers] in the layer [18] between a first contact area [FIG. 7, 13 to 14 & 24] and a second contact area [FIG. 7, 18-20] the cross-section [FIG. 7, the volume defined between the spacers] being smaller than the first contact area and the second contact area. Chiang documents a process by which spacers are formed within the opening [FIG. 4, 31] of dielectric layer 14 [page 2 section 0022].

Regarding claim 11, Chiang teaches a method as claimed in claim 10, wherein the main surface has a step profile and the step of reducing the cross-section comprises an anisotropic etching step for forming a sidewall spacer along at least a part of the step profile [page 2 section 0022].

The examiner has cited multiple reference rejections due to the multiple ways of interpreting the claims. Please note that by specifying that the "contact areas" be defined so that the electrodes are in direct and adjacent contact to the phase change material, the broad interpretations of some of the current claims might be overcome. The examiner is not insuring that claims can be overcome with such claim language. The examiner makes these comments to give the applicant further insight into the examiner's interpretations of the claims.

Allowable Subject Matter

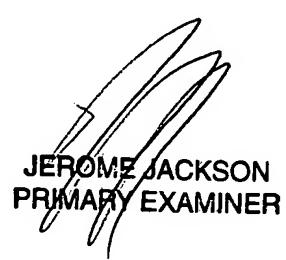
7. Claims 5,7,12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Lowrey (US Pat. Pub. 2003/0116794), Casagrande et al. (US Pat. Pub. 2006/0049391), Harshfield (US Pat. Pub. 2004/0124503), Wolstenholme (US Patent 6,236,059), Lowery et al. (US Pat. Pub. 2003/0001242) and Hudgens et al. (US Patent 6,998,289). Also see attached 892 form for these pertinent art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Budd whose telephone number 571-272-8796. The examiner can normally be reached on Monday to Friday 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



JEROME JACKSON
PRIMARY EXAMINER